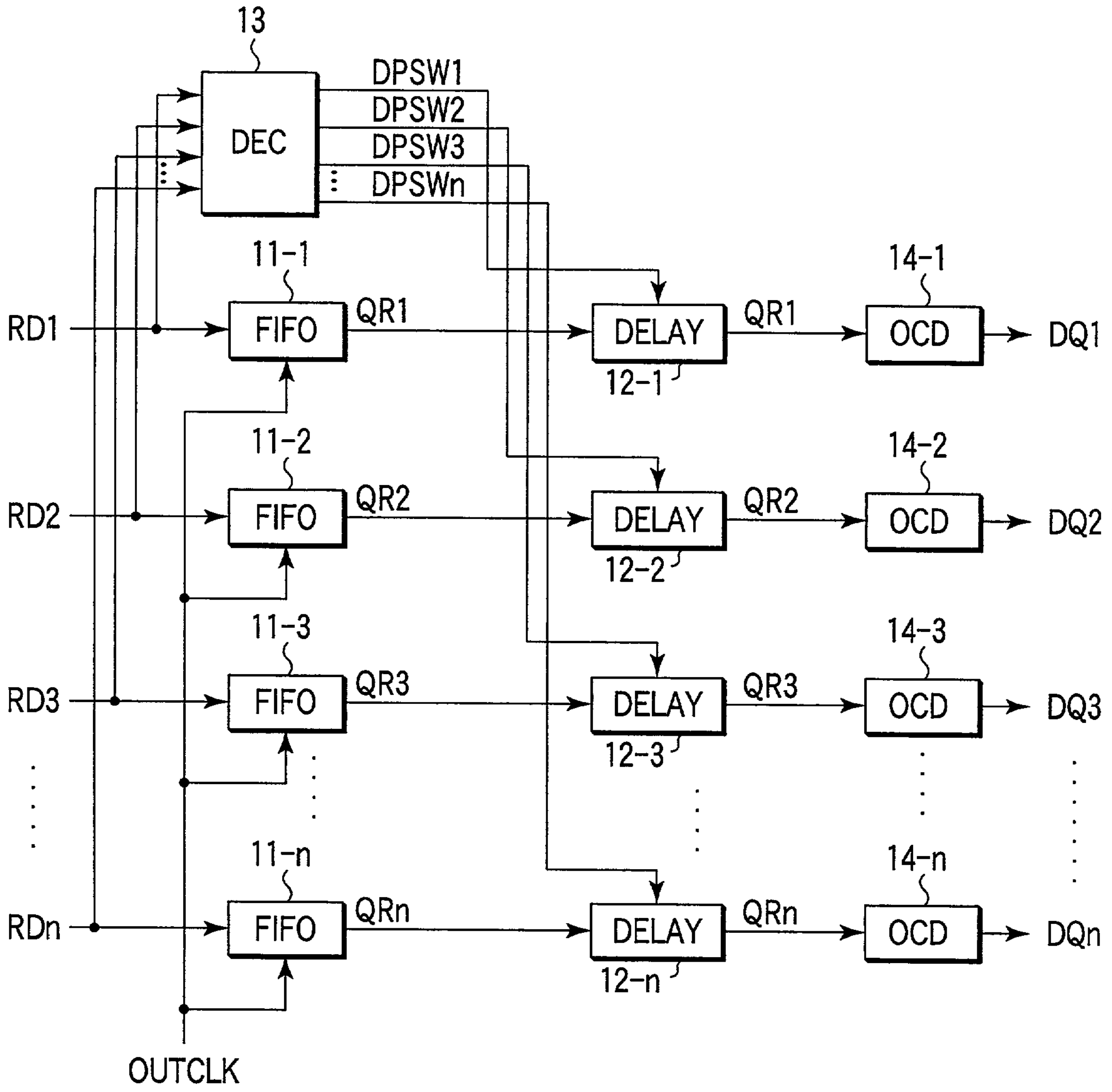

13
DEC
DPSW1
DPSW2
DPSW3
DPSWn
RD1
RD2
RD3
RDn
11-1
11-2
11-3
11-n
FIFO
FIFO
FIFO
FIFO
QR1
QR2
QR3
QRn
DELAY
DELAY
DELAY
DELAY
12-1
12-2
12-3
12-n
QR1
QR2
QR3
QRn
14-1
14-2
14-3
14-n
OCD
OCD
OCD
OCD
DQ1
DQ2
DQ3
DQn
OUTCLK

FIG. 1

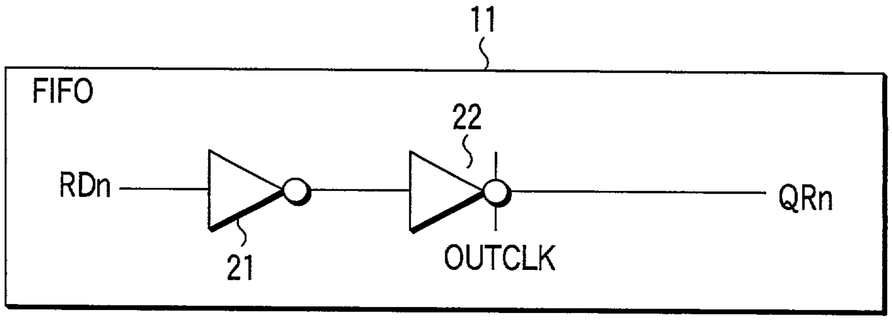

11
FIFO
22
RDn
QRn
21
OUTCLK

FIG. 2

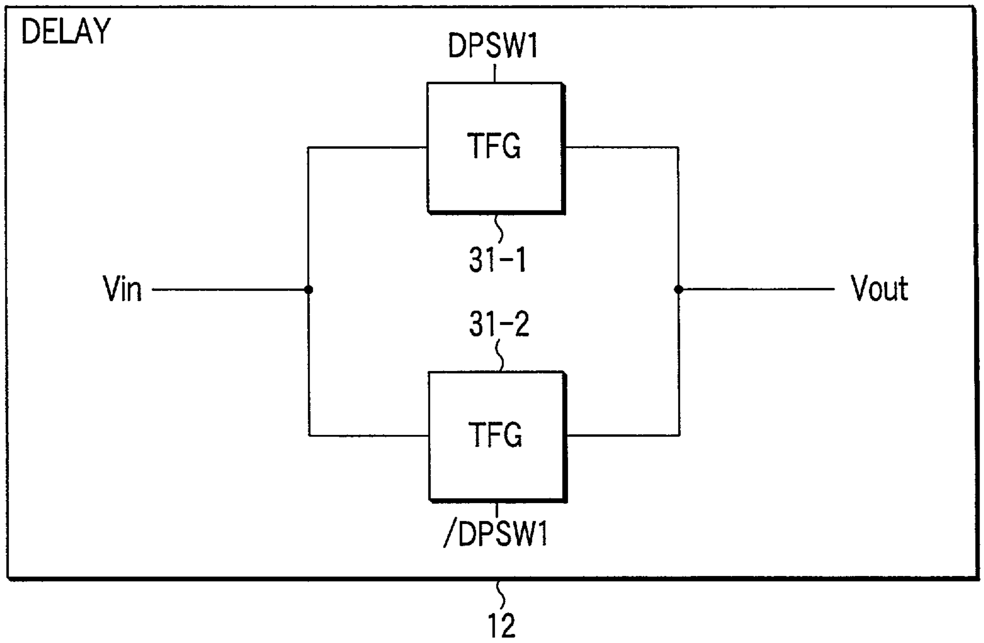

DELAY
DPSW1
TFG
31-1
Vin
Vout
31-2
TFG
/DPSW1
12

FIG. 3

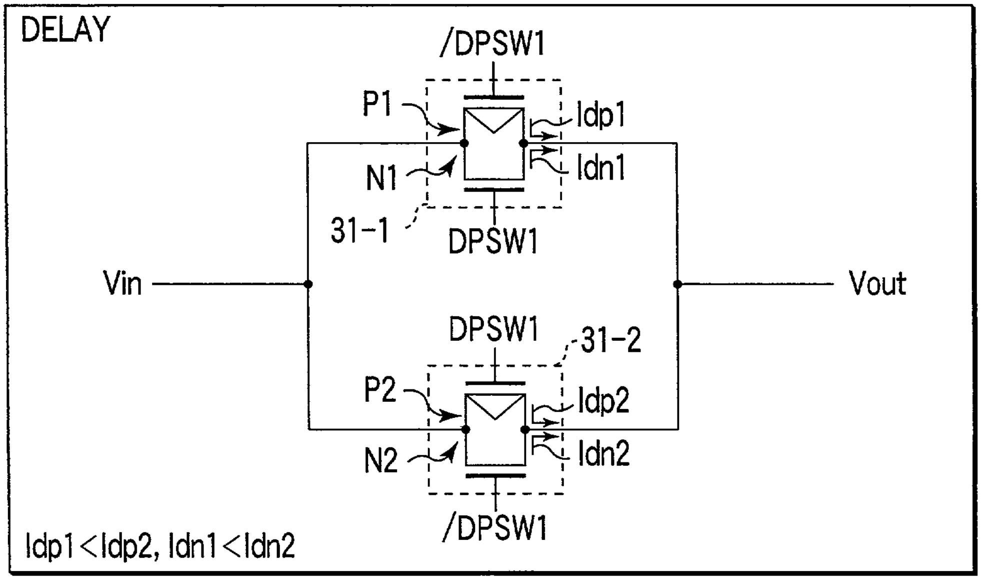
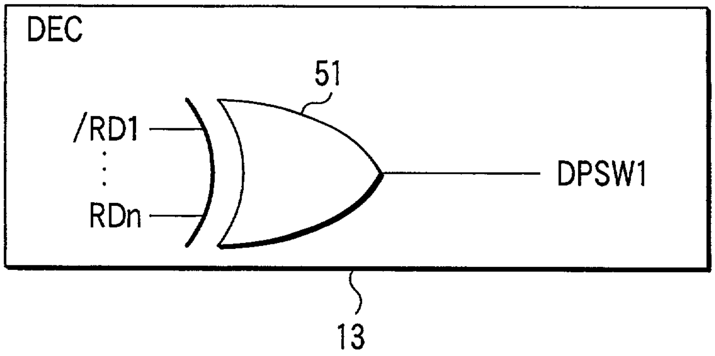
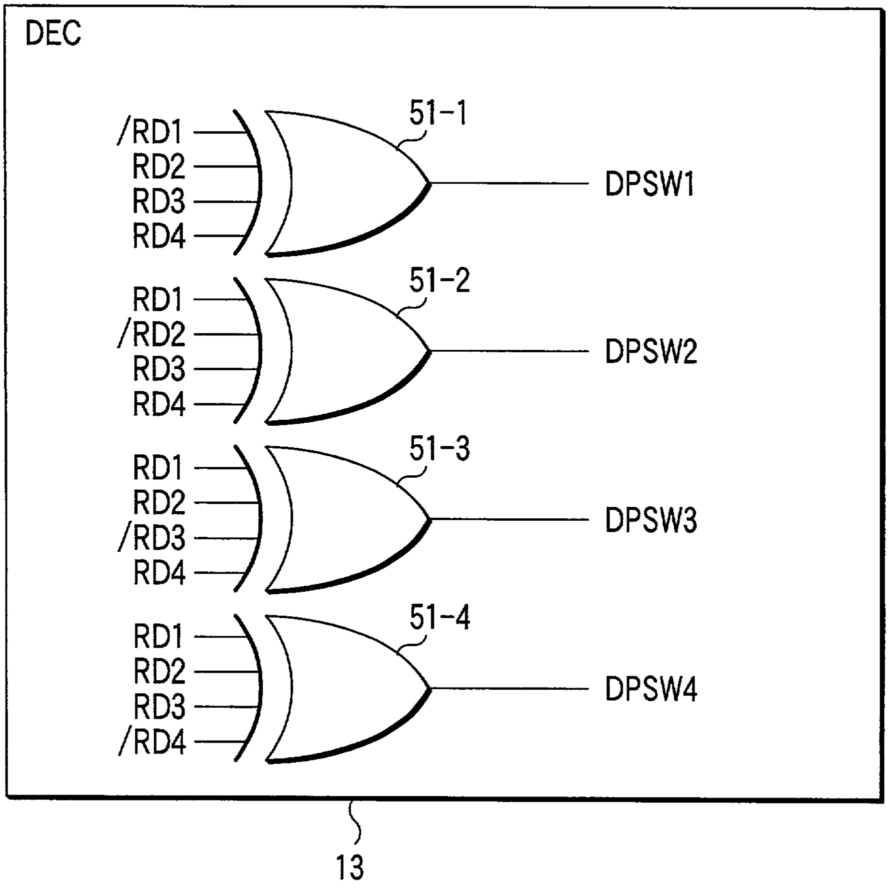

DELAY
/DPSW1
P1
Idp1
N1
Idn1
31-1
DPSW1
Vin
Vout
DPSW1
31-2
P2
Idp2
N2
Idn2
/DPSW1
Idp1<Idp2, Idn1<Idn2

FIG. 4



DEC
51
/RD1
⋮
RDn
DPSW1
13

FIG.5



DEC
51-1
/RD1
RD2
RD3
RD4
DPSW1
51-2
RD1
/RD2
RD3
RD4
DPSW2
51-3
RD1
RD2
/RD3
RD4
DPSW3
51-4
RD1
RD2
RD3
/RD4
DPSW4
13

FIG.6

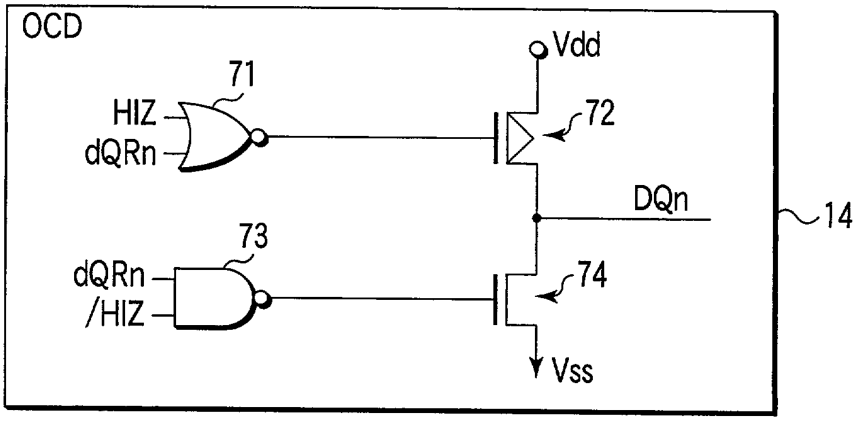

OCD
71
HIZ
dQRn
Vdd
72
DQn
14
73
dQRn
/HIZ
74
Vss

FIG. 7

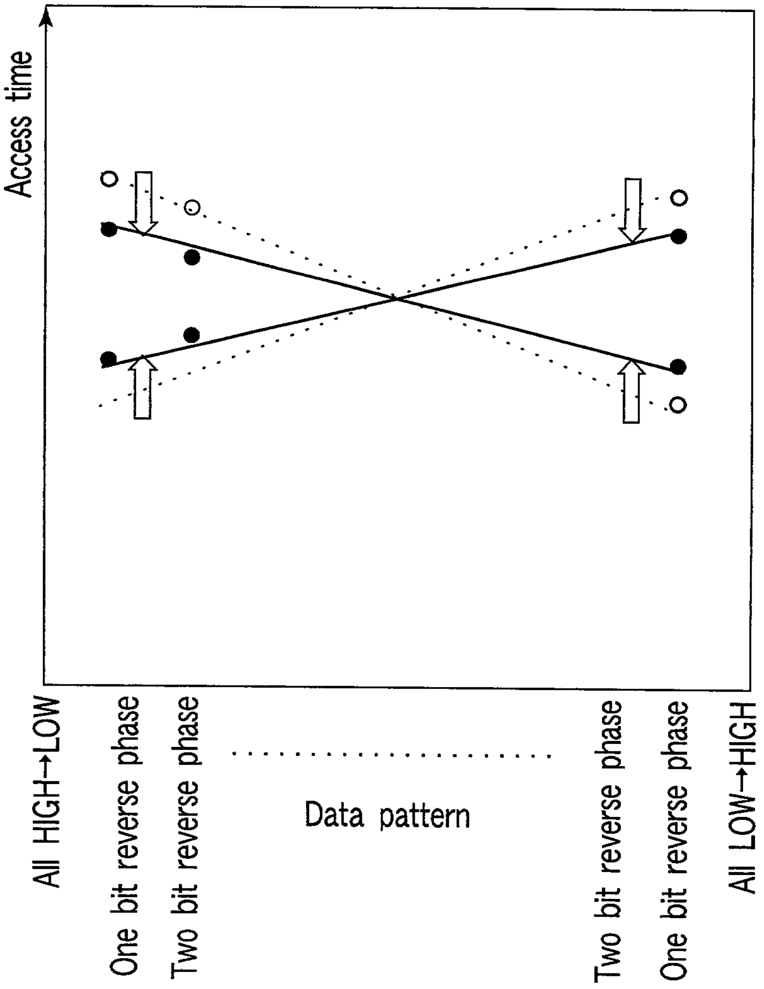
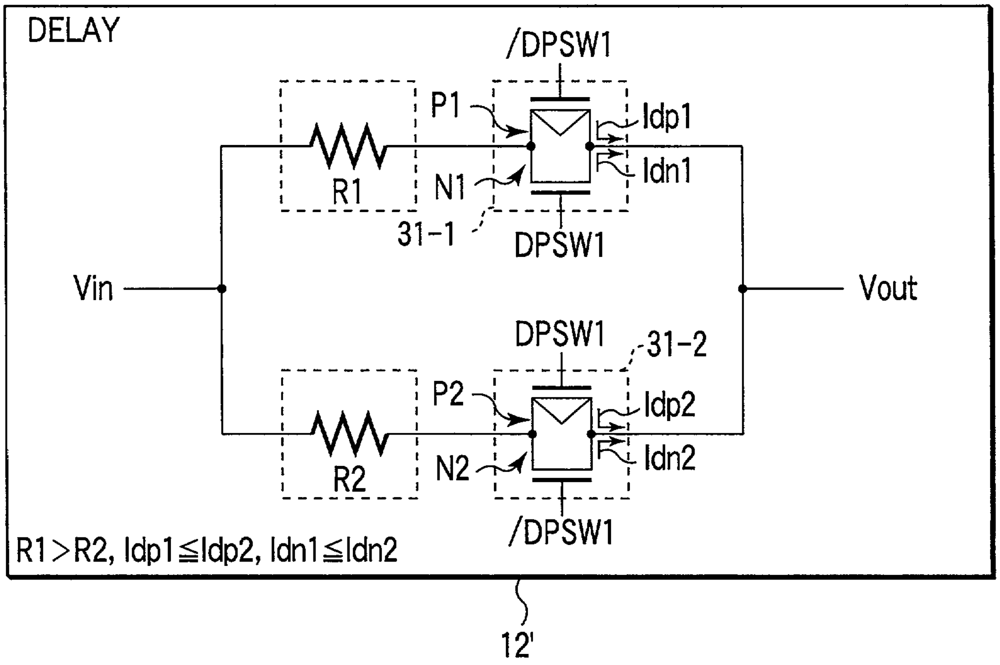
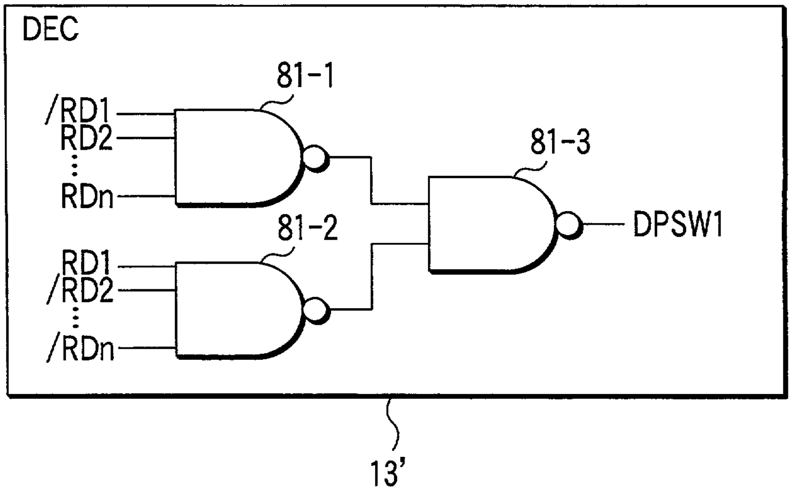

Access time
All HIGH→LOW
One bit reverse phase
Two bit reverse phase
Data pattern
Two bit reverse phase
One bit reverse phase
All LOW→HIGH

FIG. 8


DELAY
/DPSW1
P1
Idp1
R1
N1
Idn1
31-1
DPSW1
Vin
Vout
DPSW1
-31-2
P2
Idp2
N2
R2
Idn2
/DPSW1
R1>R2, Idp1≦Idp2, Idn1≦Idn2
12'

F I G. 9


DEC
81-1
/RD1
RD2
⋮
RDn
81-3
DPSW1
81-2
RD1
/RD2
⋮
/RDn
13'

F I G. 10

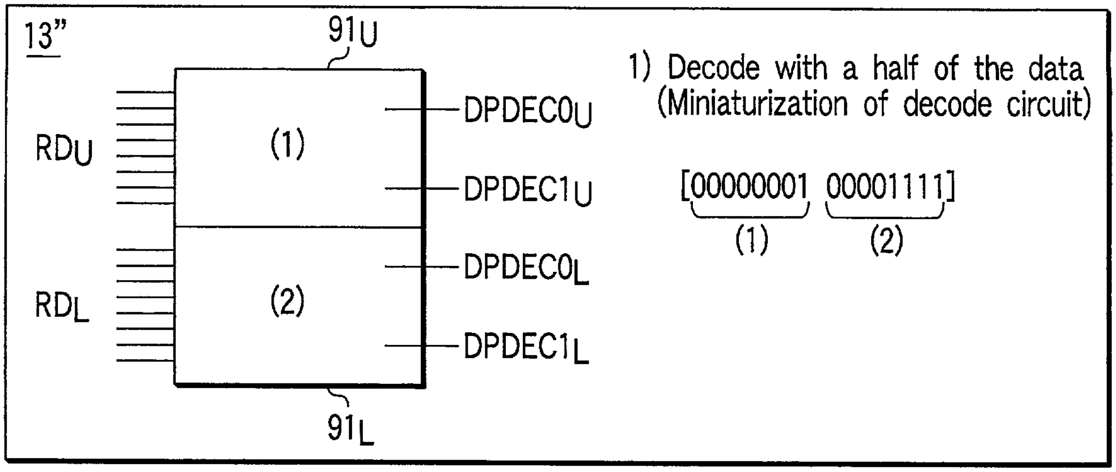


FIG. 11A

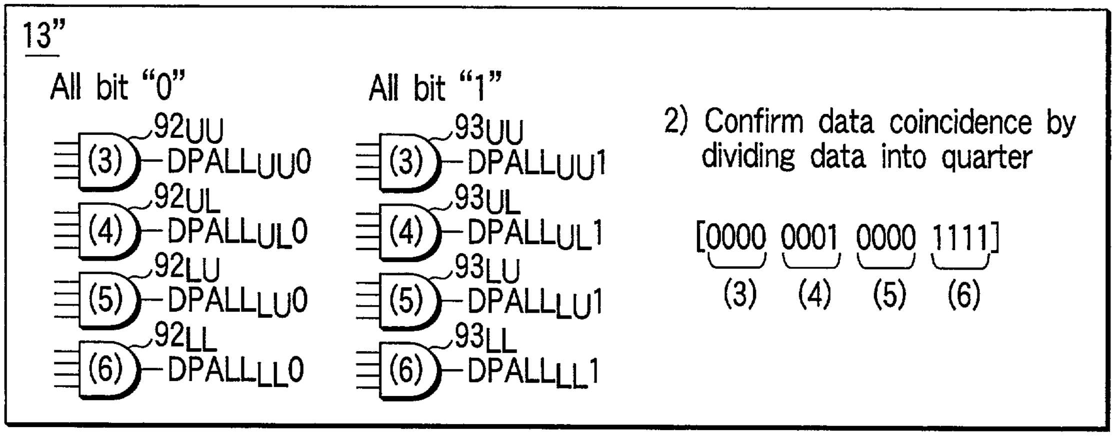


FIG. 11B

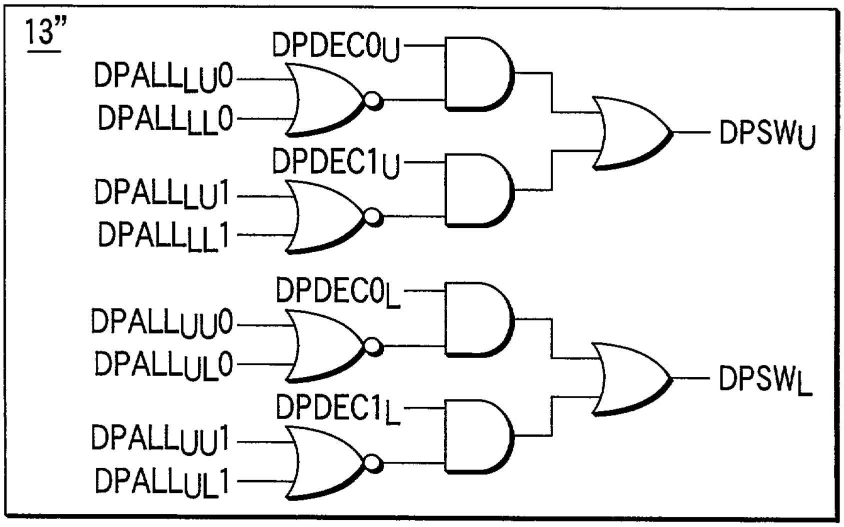
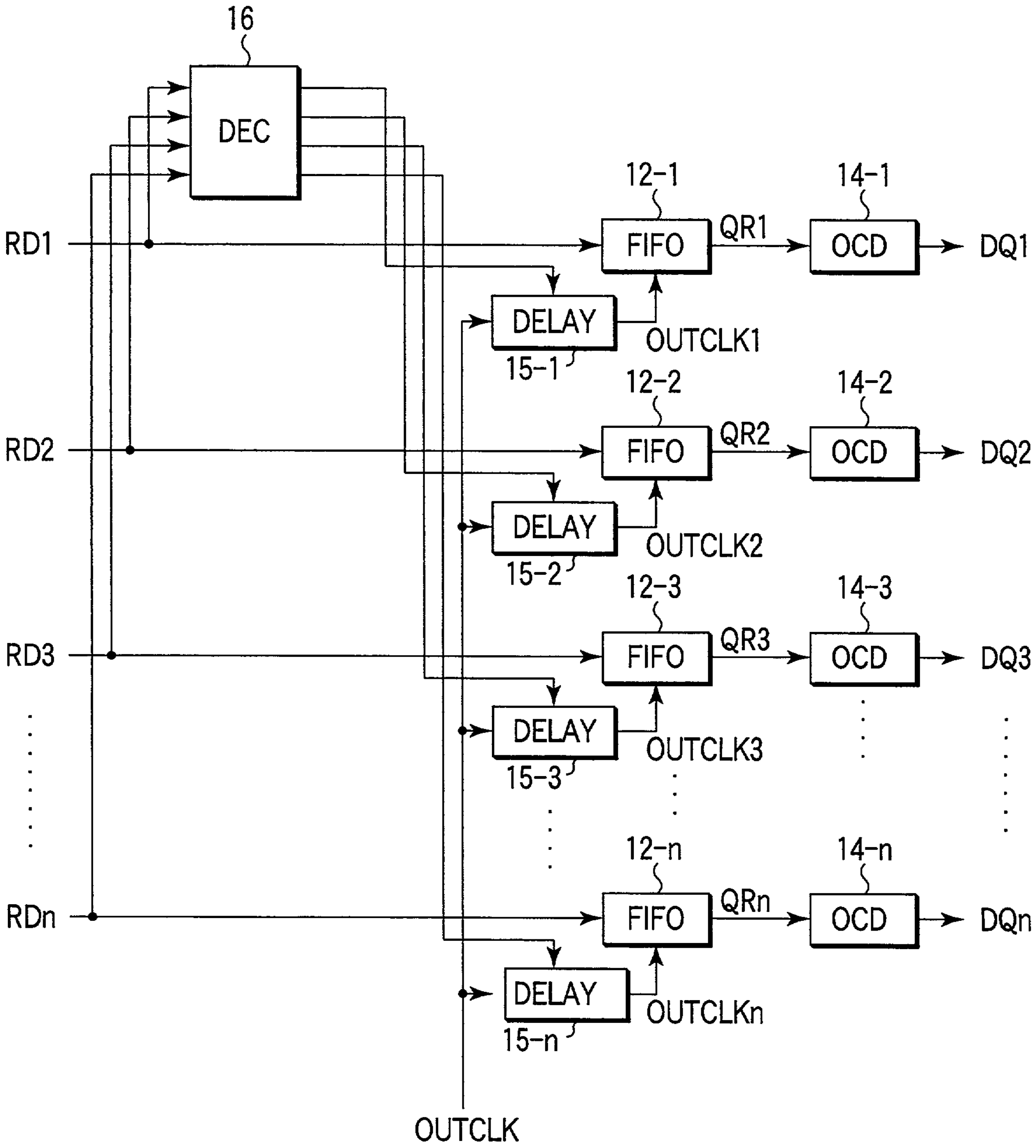


FIG. 11C


16
DEC
RD1
RD2
RD3
RDn
12-1
12-2
12-3
12-n
FIFO
FIFO
FIFO
FIFO
QR1
QR2
QR3
QRn
14-1
14-2
14-3
14-n
OCD
OCD
OCD
OCD
DQ1
DQ2
DQ3
DQn
DELAY
DELAY
DELAY
DELAY
15-1
15-2
15-3
15-n
OUTCLK1
OUTCLK2
OUTCLK3
OUTCLKn
OUTCLK

F I G. 12

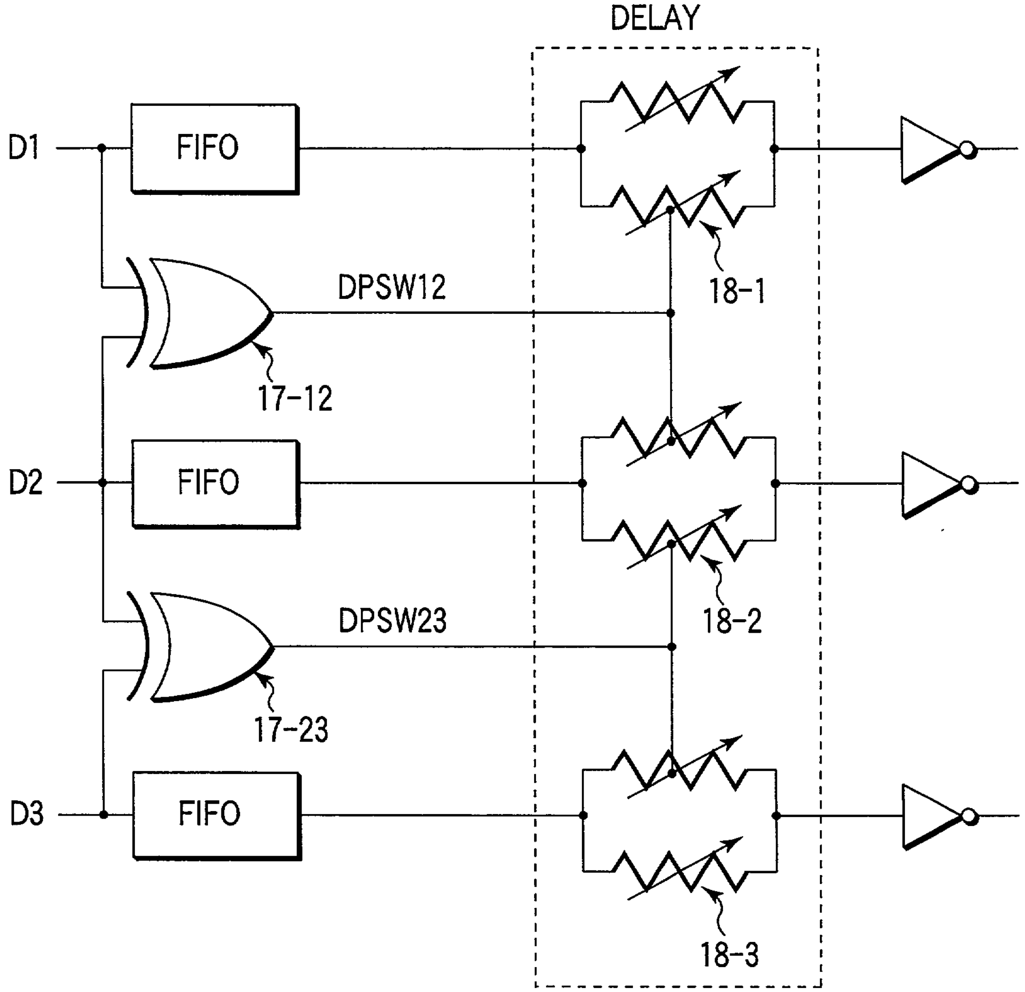


FIG. 13

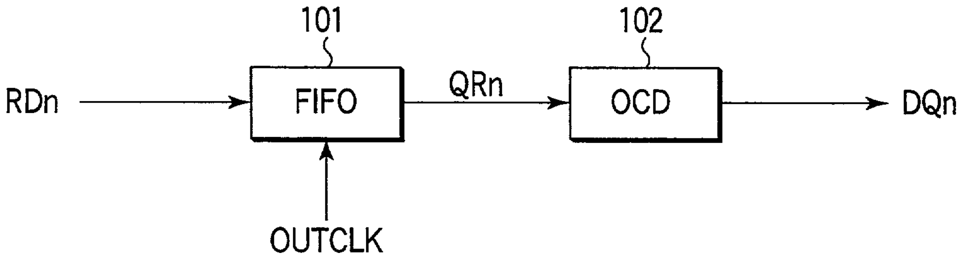


FIG. 14 PRIOR ART

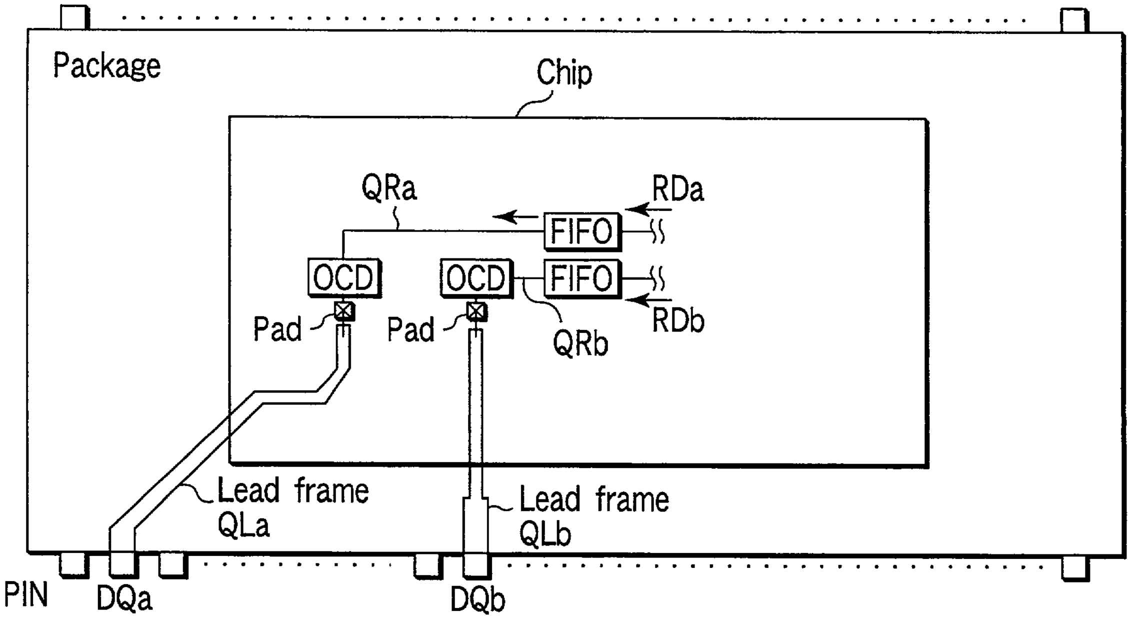


FIG. 15A PRIOR ART

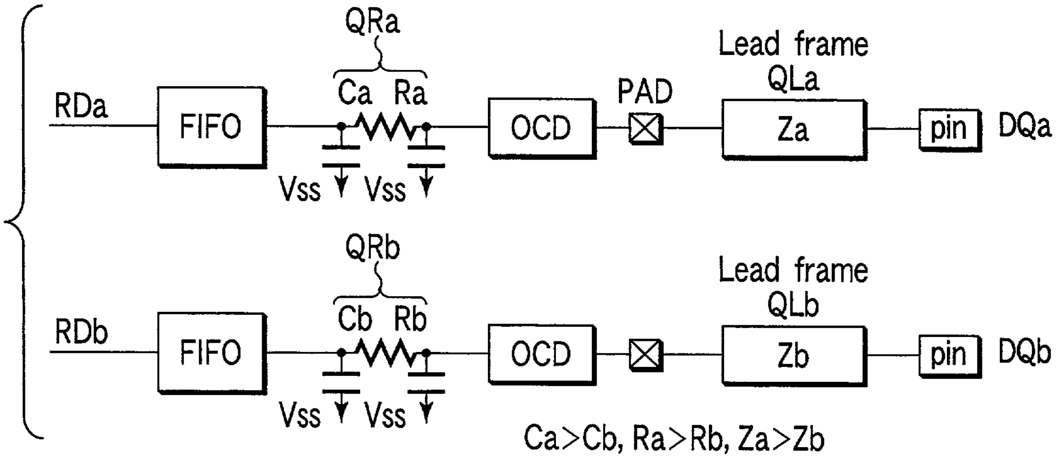
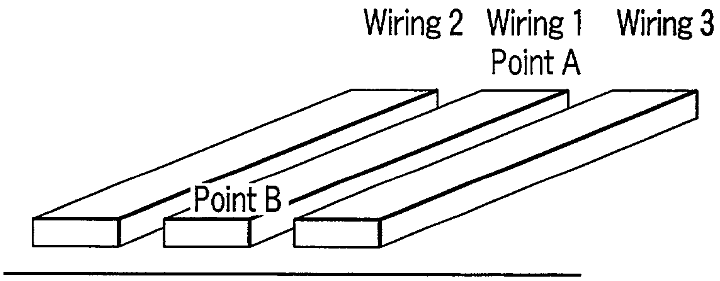
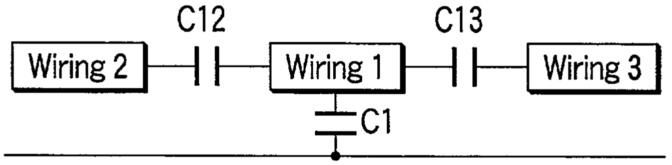


FIG. 15B PRIOR ART



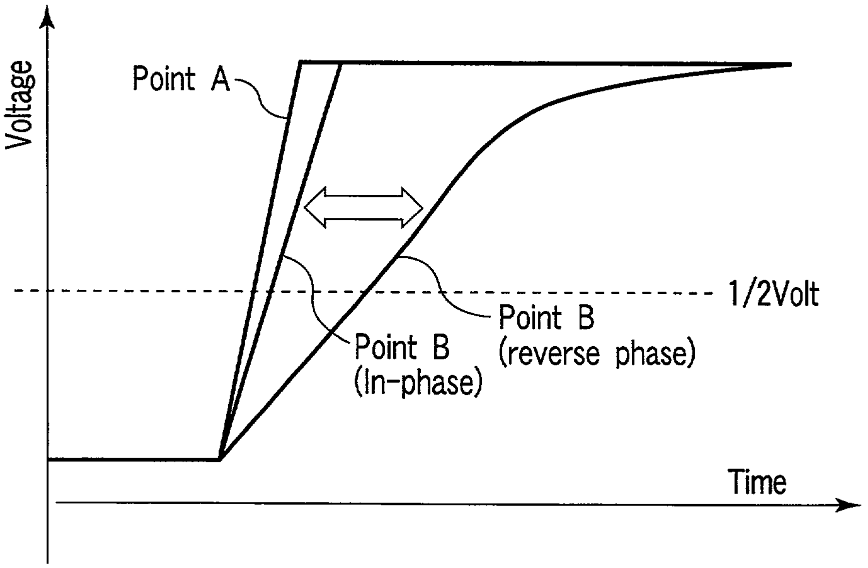
F I G. 16A
PRIOR ART



F I G. 16B
PRIOR ART

	Wiring 2	Wiring 1	Wiring 3	Data pattern
Potential change	↗	↗	↗	In-phase
	↘	↗	↘	Reverse phase
	↘	↘	↘	In-phase
	↗	↘	↗	Reverse phase

F I G. 16C
PRIOR ART



F I G. 16D
PRIOR ART

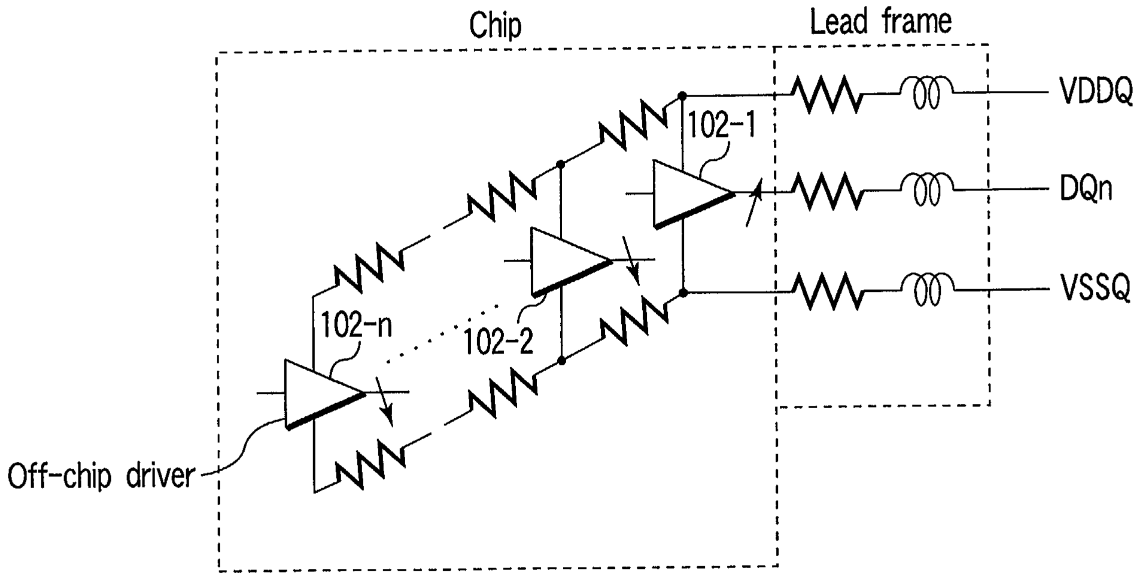
Potential change (△V) by the transient current which flows the power source GND

$$\Delta V = N \cdot Leff \cdot (di/dt)$$

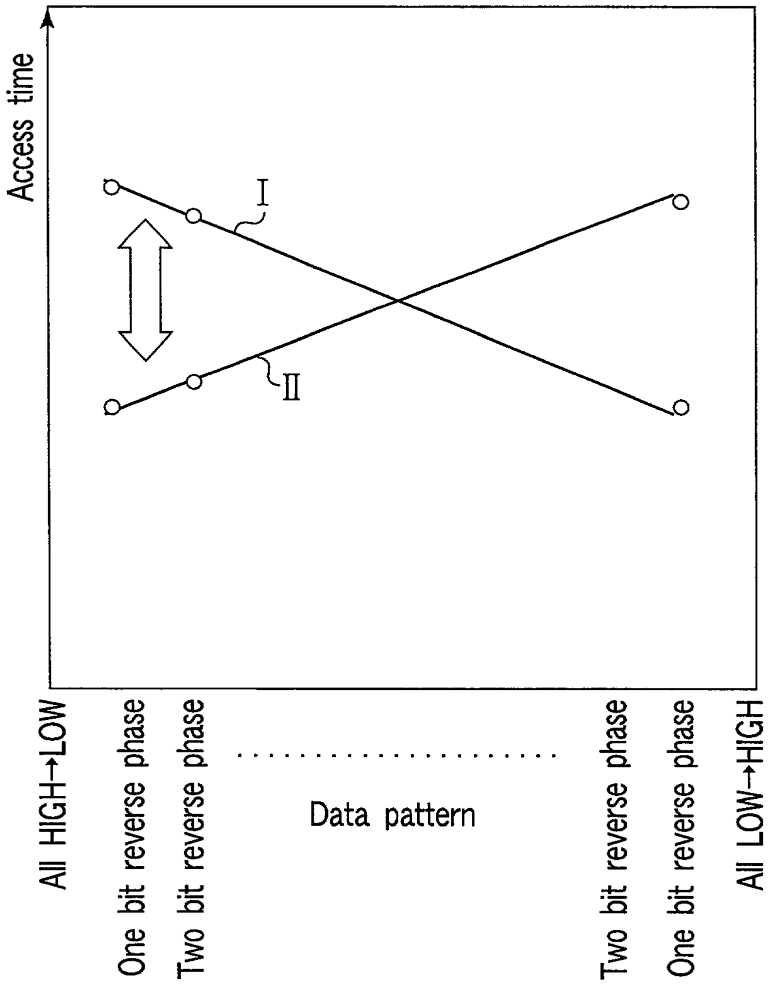
Effective inductance (Leff) of PKG (power source)

Current drive performance (di/dt) of the driver

Simultaneous switching number (N)



F I G. 17 PRIOR ART



F I G. 18 PRIOR ART